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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/519,713 | 12/30/2004 | Hidekazu Matsuura | 1204.44601X00 | 7508 |

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EXAMINER

MALDONADO, JULIO J

| ART UNIT | PAPER NUMBER |
|----------|--------------|
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2823

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/519,713

Applicant(s)

MATSUURA ET AL.

Examiner

Julio J. Maldonado

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 1-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 20060725 20041230.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 19 and 20 in the reply filed on 08/25/2006 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fjelstad (U.S. 6,856,235 B2) in view of Fukumoto et al. (U.S. 6,879,026 B2, hereinafter Fukumoto) and Lin et al. (U.S. 5,273,938, hereinafter Lin).

Fjelstad (Figs.1A-1G) teaches a method of forming a semiconductor package including providing a sacrificial layer (100) made of a conductive metallic material, a polymer material or a combination of both a conductive metallic material and a polymer material; forming wiring circuit (111, 112) on selected areas of the sacrificial layer (100); electrically connecting a semiconductor die (135) onto the surface of the wiring circuit (111, 112); molding the semiconductor die and the exposed surface of the wiring circuit (111, 112) with a molding compound (140); and removing the sacrificial layer (100) from the wiring circuit (111, 112) and the molding compound (140) (Fjelstad, column 4, line 38 – column 6, line 14).

Fjelstad fails to disclose wherein the sacrificial layer includes an adhesive layer, the adhesive film comprising a support film and a resin layer A formed on one side or both sides of the support film, the 90 degree peel strength between the resin layer A and the metal sheet prior to the processing of the metal sheet laminated with the adhesive film for semiconductor use to give the wiring circuit being 20 N/m or greater at 25°C, and the 90 degree peel strengths, after molding with a molding compound the wiring circuit laminated with the adhesive film for semiconductor use, between the resin layer A and the wiring circuit and between the resin layer A and the molding compound both being 1000 N/m or less at least one point in the temperature range of 0°C to 250°C. However, Fukumoto teaches a method of processing semiconductor devices including the steps of adhering a substrate to a sacrificial material, said sacrificial material including an adhesive layer and a support layer (Fukumoto, column 5, lines 36 – 52), wherein said adhesive layer is made of a resin manufactured by graft-copolymerizing unsaturated nitrile, alkyl (meth)acrylate, and monomer compounds, wherein said adhesive can also contain unsaturated carboxylic acid esters such as alkyl acrylate which comprises alkyl group with one to four carbons or alkyl methacrylate, preferably methyl (meth)acrylate and ethyl (meth)acrylate (Fukumoto, column 9, lines 19 – 56), and wherein the elastic modulus of said adhesive layer is of 100 MPa to 1,000 MPa (Fukumoto, column 6, lines 44 – 52); and peeling off the sacrificial layer after processing the substrate (Fukumoto, column 5, lines 19 – 35).

Furthermore, the submitted disclosure teaches wherein the adhesive material could be a resin having an ester, and wherein said adhesive has an elastic modulus of

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10 MPa or greater (Instant page 15, line 18 – page 16, line 13). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the adhesive layer of Fukumoto would also have the above-mentioned claimed properties because the layer of Fukumoto is made from the same group of materials and have overlapping properties (elastic modulus).

It would also have been within the scope of one of ordinary skill in the art to combine the teachings of Fjelstad and Fukumoto to enable the formation of the sacrificial layer of Fjelstad according to the teachings of Fukumoto because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable sacrificial layers in Fjelstad and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

The combination of Fjelstad and Fukumoto substantially teaches all aspects of the invention, but fails to disclose forming the wiring circuits by laminating a metal sheet to the sacrificial layer; and processing the metal sheet to give the wiring circuit.

However, Lin (Figs.1-3) teaches a method of forming a semiconductor package including laminating a metal sheet to a sacrificial layer (12); and processing the metal sheet to give a wiring circuit (13) (Lin, column 2, line 64 – column 3, line 24). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Fjelstad and Fukumoto with Lin to enable forming the wiring circuits of Fjelstad and Fukumoto to be performed according to the teachings of Lin because one of ordinary skill in the art at the time the invention was made would have been motivated to look to

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alternative suitable methods of forming the wiring circuits of Fjelstad and Fukumoto and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Conclusion


4. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (<http://portal.uspto.gov/external/portal/pair>) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at <http://www.uspto.gov/web/info/2800.htm>.


Julio J. Maldonado
November 7, 2006

Julio J. Maldonado
Patent Examiner
Art Unit 2823


GEORGE R. FOURSON
PRIMARY EXAMINER